

REMARKS

Claims 1-15 are currently pending in the case. Claims 1-2, 4, 6-7 and 9-14 have been amended and claims 16-22 have been canceled without prejudice.

The applicant has studied the Office Action dated December 4, 2002 and has made the changes believed appropriate to place the application in condition for allowance.

Reconsideration and reexamination are respectfully requested.

Claims 16-22 have been canceled as non-elected claims.

Applicant acknowledges with thanks the indication of allowance of Claim 15.

Claims 2-14 have been objected to as being dependent upon a rejected base claim. Claims 2, 4, 6, 7, 9, and 12-14 have been amended to independent form. It is therefore respectfully requested that the objection to claims 2-14 be withdrawn.

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over WOLF "Silicon Processing for the VLSI Era" in view of Zheng et al. "SOI bipolar-MOS merged transistors for BiCMOS application," and Schwank et al. (US Patent 6,268,630). This rejection is respectfully traversed.

Claim 1 as amended is directed to a semiconductor device comprising, *inter alia*, a field effect transistor and a bipolar transistor wherein "the first body region of the second conduction type is in contact with and thereby electrically connected to the first base region of the second conduction type ...". By contrast, the Examiner has cited no portion of the Wolf, Zheng or Schwank references which teaches or suggests, either alone or in combination such a device. Indeed, it is noted that the bipolar device of Fig. 5-75(a) of the Wolf reference cited by the Examiner appears to be isolated from the FET device by a trench. Conversely, the Zheng reference appears to be directed to a device in which a bipolar structure formed in the drain region of a MOSFET, has base and body regions which are of opposite conductivity type. The Examiner has cited no portion of the Schwank reference directed to bipolar transistors. It is therefore respectfully submitted that the rejection of claim 1 should be withdrawn.

The Examiner has made various comments concerning the obviousness of certain features of the present inventions. Applicant respectfully disagrees. Also, the Examiner's comments are deemed moot in view of the above response.

The drawings have been objected to under 37 CFR 1.83(a). This objection to the

drawings is respectfully traversed.

The Examiner has noted certain limitations and has indicated that these limitations should be shown in the drawings. It is respectfully submitted that the drawings as originally filed show the limitations of the claims. More specifically, following each limitation noted by the examiner, applicant has set forth below, as examples, citations to one or more drawings which depict the recited limitation. It is respectfully submitted that there is no requirement that all limitations of a particular claim be depicted in a single drawing. If the Examiner is aware of such a rule or regulation, the Examiner is respectfully requested to provide a citation to such a rule.

It is noted that Fig. 2 as originally filed contained typographical errors in the reference numerals. Attached is a proposed revised Fig. 2 in which the proposed changes have been marked in red for the Examiner's approval. Applicant will submit a formal drawing after approval of the amended figure.

Limitation: "the first body region of the second conduction type is electrically connected to the source region of the first conduction type."

Drawing: Fig. 2 shows body region 50a electrically connected to source region 120. In addition, Fig. 7 shows p-type body region 50a electrically connected to n-type source region 120 through p-type impurity diffusion layer 40 and contact layer 84a. Note, body region 50a is shown to be in contact with diffusion layer 40 and to be of the same conductivity type and therefore is shown to be in electrical contact with diffusion layer 40.

Limitation: "the first body region of the second conduction type is electrically connected to the first base region of the second conduction type."

Drawing: Fig. 2 shows body region 50a electrically connected to base region 220. In addition, Fig. 5 shows p-type body region 50a in contact with and therefore electrically connected to p-type base region 220.

Limitation: "the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type."

Drawing: Fig. 2 shows the drain region 130 electrically connected to the collector region 230. In addition, Fig. 5 shows the n-type drain region 130 in contact with and therefore electrically connected to n-type collector region 230.

Limitation: "the source region of the first conduction type is formed structurally isolated

from the first emitter region of the first conduction type.”

Drawing: Fig. 5 shows the source region 120 structurally isolated from the emitter region 210.

Limitation: “ the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type.”

Drawing: Fig. 2 shows the body region 54a electrically connected to the collector region 430. In addition, Fig. 11 shows the n-type body region 54a in contact with and therefore electrically connected to the n-type collector region 430.

Limitation: “ the source region of the second conduction type is electrically connected to the second collector region of the first conduction type.”

Drawing: Fig. 2 shows the source region 320 electrically connected to the collector region 430. In addition, Figs. 9 and 11 show the p-type source region 320 electrically connected to n-type collector region 430 through contact layer 84f.

Limitation: “the drain region of the second conduction type is electrically connected to the second base region of the second conduction type.”

Drawing: Fig. 2 shows the drain region 330 electrically connected to the base region 420. In addition, Fig. 11 shows the p-type drain region 330 electrically connected to the p-type base region 420 by a p-type body region 50c.

Limitation: “the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type.”

Drawing: Fig. 2 shows the collector region 230 electrically connected to the emitter region 410. In addition, Figs. 1, 5 and 11 show the n-type collector region 230 (Fig. 5) electrically connected to the n-type emitter region 410 (Fig. 11) via the contact layer 84b, wiring layer 90a, wiring Vout, wiring layer 90e and contact layer 84g.

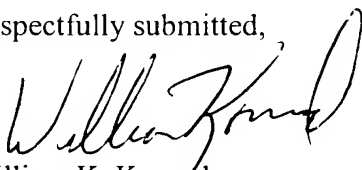
Limitation: “the first gate electrode layer is electrically connected to the second gate electrode layer.”

Drawing: Fig. 2 shows the gate electrode layer 110 electrically connected to the gate electrode layer 310. In addition, Figs. 1, 4 and 10 shows the gate electrode layer 110 (Fig. 4) electrically connected to the gate electrode layer 310 (Fig. 10) via contact layer 84d, wiring layer 90c, wiring Vin, wiring layer 90f and contact layer 84h.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is earnestly solicited.

Respectfully submitted,



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4/4/03
(Date)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 16-22 have been canceled without prejudice.

Claims 1-2, 4, 6-7 and 9-14 have been amended as follows:

1. (Amended) A semiconductor device comprising:
an insulation layer;
a semiconductor layer formed on the insulation layer;
an element isolation region formed in the semiconductor layer; and
a first element forming region and a second element forming region defined by the
element isolation region;
wherein the first element forming region includes both a first bi-polar transistor and a first
field effect transistor;
the first bi-polar transistor includes a first emitter region of a first conduction type, a first
base region of a second conduction type, and a first collector region of the first conduction type,
the first field effect transistor includes a first gate electrode layer, a source region of the
first conduction type, and a drain region of the first conduction type,
the first field effect transistor further includes a first body region of the second
conduction type formed at least between the source region of the first conduction type and the
drain region of the first conduction type,
the first body region of the second conduction type is electrically connected to the source
region of the first conduction type,
the first body region of the second conduction type is in contact with and thereby
electrically connected to the first base region of the second conduction type,
the drain region of the first conduction type is electrically connected to the first collector
region of the first conduction type, and
the source region of the first conduction type is formed structurally isolated from the first
emitter region of the first conduction type, and
wherein the second element forming region includes both a second bi-polar transistor and
a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer.

2. (Amended) A semiconductor device ~~according to claim 1~~, further comprising:
an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;

and further comprising:

a first electrode layer that continues to a side section of the first gate electrode layer and reaches the element isolation region,

wherein the first gate electrode layer is formed in a manner to cross over the element forming region,

the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer, and the element isolation region,

the drain region of the first conduction type and the collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer and the element isolation region,

the emitter region of the first conduction type is formed in a third region surrounded by the first gate electrode layer in a forming region of the first bi-polar transistor, the first electrode layer and the element isolation region, and

the first body region of the second conduction type is formed at least below the first gate electrode layer in the forming region of the first field effect transistor, and below a part of the first electrode layer.

4. (Amended) A semiconductor device ~~according to claim 1,~~ further comprising:
an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;

and further comprising:

a first layer and a second layer, wherein

the first layer has one end section continuing to the first gate electrode layer or the second layer, and another end section reaching the element isolation region,

the second layer has one end section continuing to the first gate electrode layer or the second layer, and another end section reaching the element isolation region,

the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer, the first layer and the element isolation region,

the drain region of the first conduction type and the first collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer, the second layer and the element isolation region,

the first emitter region of the first conduction type is formed in a third region surrounded by the first layer, the second layer and the element isolation region,

the first base region of the second conduction type is formed below a part of the first layer, and below a part of the second layer in the semiconductor layer, and

the first body region of the second conduction type is formed at least below the first gate electrode layer and below a part of the first layer in the semiconductor layer.

6. (Amended) A semiconductor device ~~according to claim 1, further comprising:~~
an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;

and further comprising, in the first element forming region, a second body region of the first conduction type, which is formed in the semiconductor layer between the first base region of the second conduction type and the first collector region of the first conduction type.

7. (Amended) A semiconductor device ~~according to claim 1,~~ comprising:
an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;
wherein an impurity diffusion layer of the second conduction type is further formed in the first element forming region,

wherein the impurity diffusion layer of the second conduction type is a semiconductor layer in the first region, and is formed in the semiconductor layer between the source region of the first conduction type and the first body region of the second conduction type, and

the source region of the first conduction type and the first body region of the second conduction type are electrically connected to one another through the impurity diffusion layer of the second conduction type.

9. (Amended) A semiconductor device ~~according to claim 1~~, comprising:
an insulation layer;
a semiconductor layer formed on the insulation layer;
an element isolation region formed in the semiconductor layer; and
a first element forming region and a second element forming region defined by the
element isolation region;
wherein the first element forming region includes both a first bi-polar transistor and a first
field effect transistor;
the first bi-polar transistor includes a first emitter region of a first conduction type, a first
base region of a second conduction type, and a first collector region of the first conduction type,
the first field effect transistor includes a first gate electrode layer, a source region of the
first conduction type, and a drain region of the first conduction type,
the first field effect transistor further includes a first body region of the second
conduction type formed at least between the source region of the first conduction type and the
drain region of the first conduction type,
the first body region of the second conduction type is electrically connected to the source
region of the first conduction type,
the first body region of the second conduction type is electrically connected to the first
base region of the second conduction type,
the drain region of the first conduction type is electrically connected to the first collector
region of the first conduction type, and
the source region of the first conduction type is formed structurally isolated from the first
emitter region of the first conduction type, and
wherein the second element forming region includes both a second bi-polar transistor and
a second field effect transistor,
the second bi-polar transistor includes a second emitter region of the first conduction
type, a second base region of the second conduction type, and a second collector region of the
first conduction type,
the second field effect transistor includes a second gate electrode layer, a source region of
the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;
and

wherein a third body region of the second conduction type is formed in the semiconductor layer between the first collector region of the first conduction type and the first emitter region of the first conduction type and in the semiconductor layer adjacent to the element isolation region.

10. (Amended) A semiconductor device according to ~~any one of~~ claim 8, wherein a contact layer for electrically connecting the source region of the second conduction type and the second contact region of the first conduction type is formed in the second element isolation region, wherein the contact layer is formed in a manner to cross over the source region of the second conduction type and the second collector region of the first conduction type.

11. (Amended) A semiconductor device according to ~~any one of~~ claim 9, wherein a fourth body region of the second conduction type is formed in the semiconductor layer between the second collector region of the first conduction type and the second emitter region of the first conduction type, and in the semiconductor layer adjacent to the element isolation region.

12. (Amended) A semiconductor device ~~according to claim 1,~~ comprising:

an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;
and

wherein the first conduction type is n-type, and the second conduction type is p-type.

13. (Amended) A semiconductor device ~~according to claim 1,~~ comprising:
an insulation layer;

a semiconductor layer formed on the insulation layer;

an element isolation region formed in the semiconductor layer; and

a first element forming region and a second element forming region defined by the element isolation region;

wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor;

the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type,

the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type,

the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type,

the first body region of the second conduction type is electrically connected to the source region of the first conduction type,

the first body region of the second conduction type is electrically connected to the first base region of the second conduction type,

the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and

the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and

wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor,

the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type,

the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;
and

wherein the first conduction type is p-type, and the second conduction type is n-type.

14. (Amended) A semiconductor device ~~according to claim 1~~, comprising:
an insulation layer;
a semiconductor layer formed on the insulation layer;
an element isolation region formed in the semiconductor layer; and
a first element forming region and a second element forming region defined by the
element isolation region;
wherein the first element forming region includes both a first bi-polar transistor and a first
field effect transistor;
the first bi-polar transistor includes a first emitter region of a first conduction type, a first
base region of a second conduction type, and a first collector region of the first conduction type,
the first field effect transistor includes a first gate electrode layer, a source region of the
first conduction type, and a drain region of the first conduction type,
the first field effect transistor further includes a first body region of the second
conduction type formed at least between the source region of the first conduction type and the
drain region of the first conduction type,
the first body region of the second conduction type is electrically connected to the source
region of the first conduction type,
the first body region of the second conduction type is electrically connected to the first
base region of the second conduction type,
the drain region of the first conduction type is electrically connected to the first collector
region of the first conduction type, and
the source region of the first conduction type is formed structurally isolated from the first
emitter region of the first conduction type, and
wherein the second element forming region includes both a second bi-polar transistor and
a second field effect transistor,
the second bi-polar transistor includes a second emitter region of the first conduction
type, a second base region of the second conduction type, and a second collector region of the
first conduction type,
the second field effect transistor includes a second gate electrode layer, a source region of
the second conduction type, and a drain region of the second conduction type,

the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type,

the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type,

the source region of the second conduction type is electrically connected to the second collector region of the first conduction type,

the drain region of the second conduction type is electrically connected to the second base region of the second conduction type,

the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and

the first gate electrode layer is electrically connected to the second gate electrode layer;
and

wherein the semiconductor layer is a silicon layer.